

ABSTRACT OF THE DISCLOSURE

A timing adjustment device, method and chip for a bus interface. Through repetitive adjustment of the amount of phase shift in the clocking signal to the bus interface, read/write testing of the bus interface and checking for the correctness of the 5 read/write data, suitability of the phase shift in the memory bus clocking signal for operating normally is determined. Hence, a safety range for the amount of phase shift in the bus interface timing signal is found and the phase shift of the bus interface timing signal is set to the mid-point of the safety range. The method may also be applied to a system bus and the timing adjustment of signals between a control chipset bus and a 10 memory bus.

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